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JCSB U.S. PTO
09/703181



17	Subclass
716	Class
ISSUE CLASSIFICATION	

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PATENT NUMBER

U.S. UTILITY Patent Application

12W SCANNED	O.I.P.E. 333	PATENT DATE 1/10/00
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APPLICATION NO. 09/703181	CONT/PRIOR	CLASS 326 327 716	SUBCLASS 39 17	ART UNIT 2819 3825	EXAMINER L. KIK
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APPLICANTS

Michael Moore
James Lie

TITLE

Architecture for efficient implementation of serial data communication functions on a programmable logic device (PLD)

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
716	17	716	100				
INTERNATIONAL CLASSIFICATION		327	149				
G06F	17/50	326	38	39			
G06F	13/00						
G06F	7/38						
H03L	7/06						

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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. 4	Figs. Drwg. 7	Print Fig. 1	Total Claims 23	Print Claim for O.G. 1
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	ANDREA LHM (Assistant Examiner)			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____				ISSUE FEE	
	(Primary Examiner)			Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	(Legal Instruments Examiner)			ISSUE BATCH NUMBER	

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